REMARKS/ARGUMENTS

1. Rejection of claims 1-4, 6-8, 10-12, 14-16, 18, and 20-28 under 35 U.S.C. 102(e):

Claims 1-4, 6-8, 10-12, 14-16, 18, and 20-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US 6,671,325).

Response:

The applicant would like to point out how the pending claims are patentable over Lee.

Claim 1 contains the limitation of "a digital-signal-format transformer electrically connected to the signal-selecting device for transforming the first digital audio signal or the second digital audio signal into a pulse audio signal".

On the other hand, Lee does not teach transforming a digital audio signal into a pulse audio signal as claimed. Lee teaches in Figure 4 and in column 13 lines 55-62 that the Reed-Solomon Error Correction Encoder 420 is used for adding error correction codes to audio data samples. The Reed-Solomon Error Correction Encoder 420 is not used for transforming a digital audio signal into a pulse audio signal, as is recited in claim 1.

Claim 1 also contains the limitation of "a synthesizing module electrically connected to the digital-signal-format transformer for merging the control signal and the pulse audio signal into a digital signal of bit-stream form".

However, Lee does not teach merging a control signal and the pulse audio into a digital signal of bit-stream form. Instead, Lee teaches a clock circuit 440 used for providing necessary timing signals to the analog-to-digital converters 315 and 320 to ensure the fixed rate of 48 kHz (column 14, lines 60-67). The

clock signals provided by the clock circuit 440 are of a fixed frequency, and do not represent a control signal. Furthermore, the clock signals are not merged with any pulse audio signal by the frame formatter 425. The frame formatter 425 merely appends timing preambles and start flag signals to each transmit frame of digitized samples of the analog signals (column 14, lines 1-8). Therefore, the frame formatter 425 does not merge a control signal with a pulse audio signal to create a digital signal of bit-stream form, as is claimed. Therefore, for the above reasons, claim 1 is patentable over the cited prior art.

Similarly, **claim** 7 contains the limitation "a separating module electrically connected to the demodulation module for separating the digital signal of bit-stream form into a control signal and a pulse audio signal".

Lee teaches a receive data buffer controller 515 for receiving demodulated digitized samples from the demodulator 510. However, the receive data buffer controller 515 does not separate a digital signal of bit-stream form into a control signal and a pulse audio signal. Lee states from column 16, line 65 to column 17, line 4 that "The receiving clocking circuit 560 provides the oversampling timing signal to the receiver 505 to recover the modulated carrier signal and to lock the receiving system 300 to ensure the recovery of the modulated carrier signal. As described prior, the receiving clock circuit 560 is nominally identical to the clock of the transmitting system 440 of FIG. 4." The clock produced by the receiving clocking circuit 560 is produced independently of the receive data buffer controller 515, so it cannot be said that the receive data buffer controller 515 separates the clock signal from the demodulated digitized samples from the demodulator 510.

Claim 7 also contains the limitation of "a digital-signal-format transformer electrically connected to the separating module for

transforming the pulse audio signal into a digital audio signal".

Similar to the Reed-Solomon Error Correction Encoder 420 disclosed above, Lee teaches a Reed-Solomon ECC decoder 525 that checks and corrects the most significant bytes of designated digitized samples using the Reed-Solomon ECC method (column 15, lines 44-53). Therefore, Lee does not teach that the Reed-Solomon ECC decoder 525 transforms a pulse audio signal into a digital audio signal, as is recited in claim 7. For the above reasons, the applicant submits that claim 7 is patentable over the cited prior art.

Like claim 7, **claim 10** contains limitations of both "a separating module for separating the digital signal of bit-stream form into a control signal and a pulse audio signal" and "a digital-signal-format transformer electrically connected to the separating module for transforming the pulse audio signal into a digital audio signal". As was explained above with respect to claim 7, Lee does not teach these claimed limitations, and claim 10 is patentable over the cited prior art.

Similar to claim 1, **claim 15** contains the limitations of "a digital-signal-format transformer electrically connected to the signal-selecting device for transforming the first digital audio signal or the second digital audio signal into a pulse audio signal" and a synthesizing module electrically connected to the digital-signal-format transformer for merging the control signal and the pulse audio signal into a digital signal of bit-stream form". As was explained above with respect to claim 1, Lee does not teach these claimed limitations, and claim 15 is patentable over the cited prior art.

Like claims 1 and 7, **claim 18** contains the limitations of "a selecting-synthesizing device for transforming the first digital audio input

signal into a transformed digital audio signal and then for merging the transformed digital audio signal with the control input signal to generate a digital input signal of bit-stream form" and "a separating-classifying device for separating the digital output signal of bit-stream form into a control output signal and a first digital audio output signal". Since Lee does not teach either of these claimed limitations, claim 18 is patentable over the cited prior art.

Similar to claim 1, **claim 25** contains the limitations of "a digital-signal-format transformer electrically connected to the signal-selecting device for transforming the first digital audio input signal or the second digital audio input signal into a pulse audio signal" and "a synthesizing module electrically connected to the digital-signal-format transformer for merging the control input signal and the pulse audio signal into the digital input signal of bit-stream form". As was explained above with respect to claim 1, Lee does not teach these claimed limitations, and claim 25 is patentable over the cited prior art.

Like claim 7, **claim 27** contains limitations of both "a separating module for separating the digital output signal of bit-stream form into the control output signal and the pulse audio signal" and "a digital-signal-format transformer electrically connected to the separating module for transforming the pulse audio signal into the digital audio output signal". As was explained above with respect to claim 7, Lee does not teach these claimed limitations, and claim 27 is patentable over the cited prior art.

Furthermore, claims 2-4, 6-8, 11-12, 14-16, and 20-28 are dependent on claims 1, 10, and 18, and should be allowed if their respective base claims are allowed. Reconsideration of claims 1-4, 6-8, 10-12, 14-16, 18, and 20-28 is therefore respectfully requested.

2. Rejection of claims 5, 9, 13, 17, 19, and 29 under 35 U.S.C. 103(a):

Claims 5, 9, 13, 17, 19, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6,671,325) in view of KHAYRALLAH et al. (US 2001/0044294).

Response:

Claims 5, 9, 13, 17, 19, and 29 are dependent on claims 1, 10, and 18, and should be allowed if their respective base claims are allowed. Reconsideration of claims 5, 9, 13, 17, 19, and 29 is therefore respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)